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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,064	10/14/2003	Peter Weitz	MUH-12823	4356
24131	7590	07/13/2004		EXAMINER
LERNER AND GREENBERG, PA				NGUYEN, KHIEM D
P O BOX 2480				
HOLLYWOOD, FL 33022-2480			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/685,064	PETER WEITZ
	Examiner Khiem D Nguyen	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 October 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1 and 2 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 October 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>110703</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Li et al. (U.S. Patent 6,627,530).

In re claim 1, AAPA discloses a method for writing to magnetoresistive memory cells, which comprises (Background of the Invention on pages 1-2 and **FIG. 2** (PRIOR ART) of this application): providing an integrated magnetoresistive semiconductor memory configuration having MRAM memory cells (**FIG. 2: 10**) located at crossover points between first selection lines (**FIG. 2: 5**) embedded in a first line plane (**FIG. 2: 1**) directly contacting the MRAM memory cells and second selection lines (**FIG. 2: 6**) embedded in a second line plane (**FIG. 2: 2**) directly contacting the MRAM memory cells, the second line plane being separate from the first line plane (**FIG. 2**), the first selection lines and the second selection lines for impressing read/write currents (**FIG. 2: I1 and I2**) for writing information items to the MRAM memory cells and for impressing read/write currents for reading the information items from the MRAM memory cells (page 2, lines 2-19).

AAPA does not explicitly disclose providing the integrated magnetoresistive semiconductor memory configuration with a third line plane being spatially separated and

electrically isolated from the first line plane and the second line plane; providing the third line plane with write selection lines for writing a cell information item; providing the integrated magnetoresistive semiconductor memory configuration with a fourth line plane being spatially separated and electrically isolated from the first line plane, the second line plane, and the third line plane; providing the fourth line plane with write selection lines for writing a cell information item; impressing a main write current in a direction through one of the write selection lines in the third line plane and through one plane for writing to a particular one of the MRAM cells, while also impressing an additional write current through one of the first selection lines adjoining the particular one of MRAM the write selection lines in the fourth line memory cells and through one of the second selection lines adjoining the particular one of MRAM memory cells; and when impressing the additional write current, impressing the additional write current being small compared to the main write current and in the same direction as the main write current.

Li discloses providing the integrated magnetoresistive semiconductor memory configuration with a third line plane (**FIG. 8: 166A and 166B**) being spatially separated and electrically isolated from the first line plane (**FIG. 8: 146A and 146B**) and the second line plane (**FIG. 8: 126A and 126B**); providing the third line plane with write selection lines for writing a cell information item; providing the integrated magnetoresistive semiconductor memory configuration with a fourth line plane (**FIG. 8: 106A and 106B**) being spatially separated and electrically isolated from the first line plane (**FIG. 8: 146A and 146B**), the second line plane (**FIG. 8: 126A and 126B**), and the third line plane (**FIG. 8: 166A and 166B**); providing the fourth line plane with write

selection lines for writing a cell information item (col. 7, line 11 to col. 9, line 30 and **FIGS. 6-8**); impressing a main write current in a direction through one of the write selection lines in the third line plane and through one of the write selection lines in the fourth line plane for writing to a particular one of the MRAM cells, while also impressing an additional write current through one of the first selection lines adjoining the particular one of MRAM memory cells and through one of the second selection lines adjoining the particular one of MRAM memory cells; and when impressing the additional write current, impressing the additional write current being small compared to the main write current and in the same direction as the main write current (col. 8, line 66 to col. 9, line 30 and **FIG. 8**). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Li to enable the third and fourth line planes of AAPA to be formed and furthermore to obtain a three dimensional memory array having a desired number of memory levels (col. 8, line 66 to col. 9, line 11).

In re claim 2, AAPA discloses wherein the method according to claim 1, which further comprises: when impressing the additional write current, setting a current intensity of the additional write current such that a maximum voltage drop is established along the one of the first selection lines (**FIG. 2: 5**) adjoining the particular one of MRAM memory cells and along the one of the second selection lines adjoining the particular one of MRAM memory cells; defining a current-voltage characteristic curve of the particular one of MRAM memory cells such that the current- voltage characteristic curve has a region of high resistance and a region of low resistance; and ensuring that the

maximum voltage drop lies in the region of high resistance in the current-voltage characteristic curve of the particular one of MRAM memory cells (Background of the Invention, pages 1-2 and **FIG. 2 (PRIOR ART)**).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



K.N.
July 11, 2004

**W. DAVID COLEMAN
PRIMARY EXAMINER**